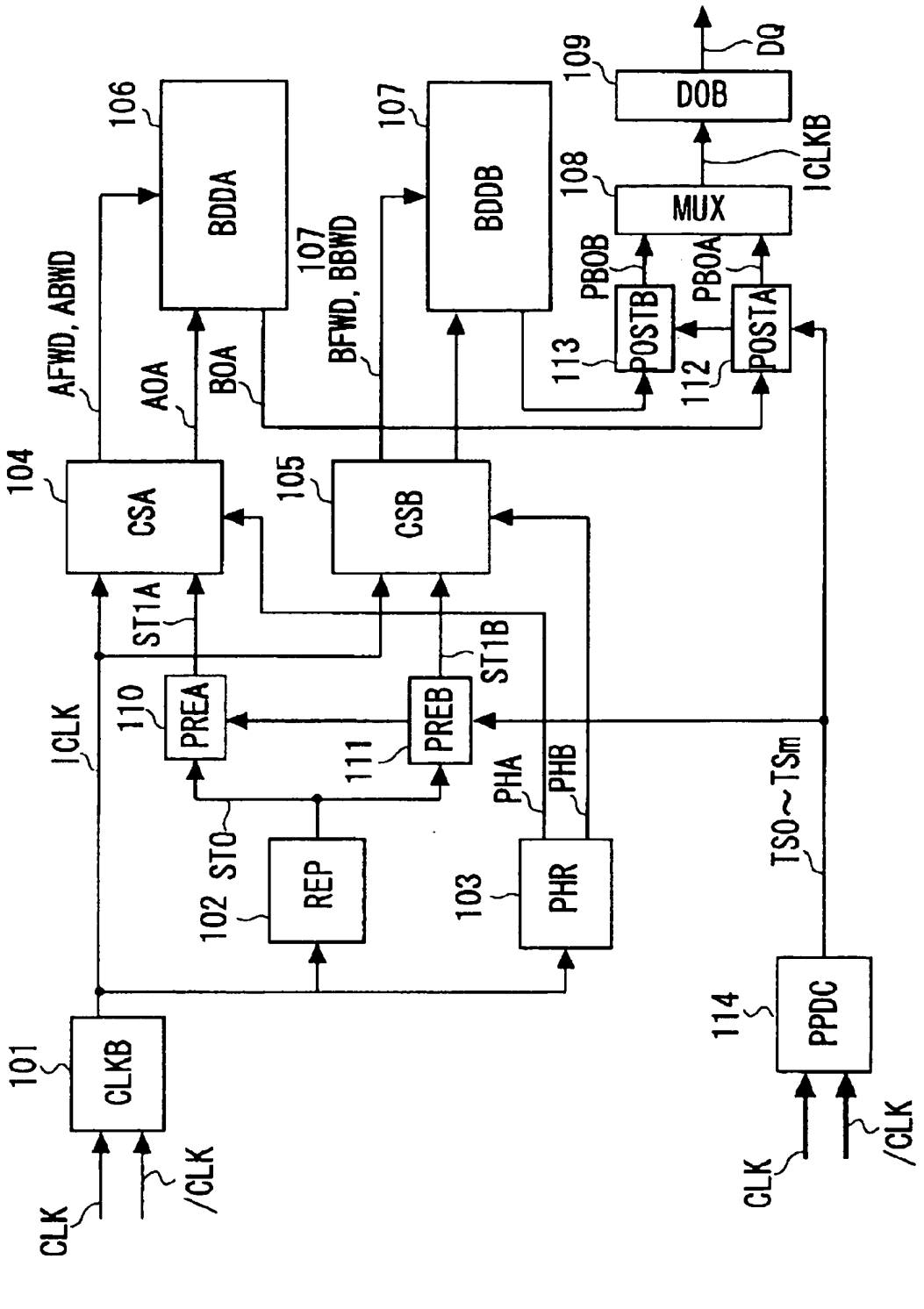

CLK
/CLK
101
CLKB
ICLK
102 STO
REP
103
PHR
PHA
PHB
TSO~TSm
114
PPDC
CLK
/CLK
110
PREA
111
PREB
ST1A
ST1B
104
CSA
105
CSB
AFWD, ABWD
AOA
BOA
BFWD, BBWD
106
BDDA
107
BDDB
107
113
POSTB
112
POSTA
PBOB
PBOA
108
MUX
ICLKB
109
DOB
DQ

FIG. 1

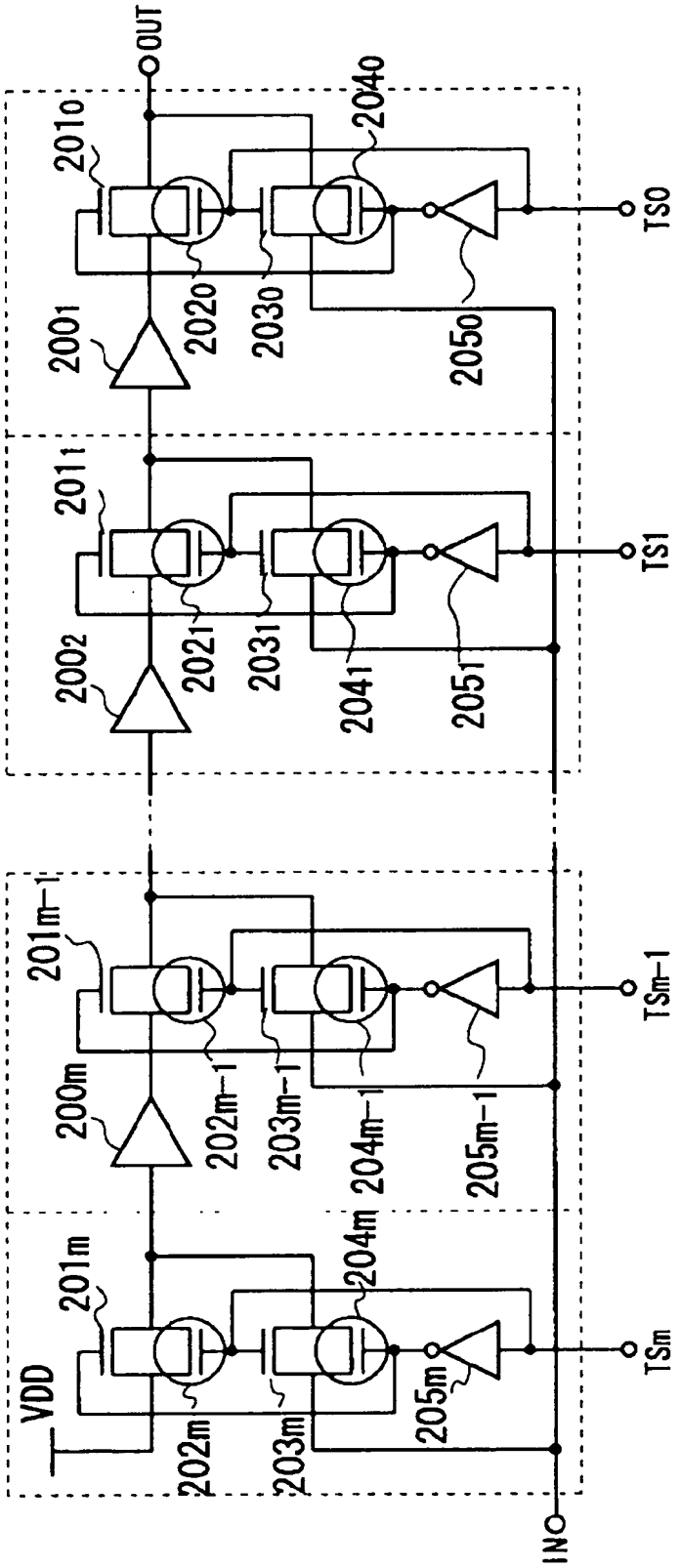
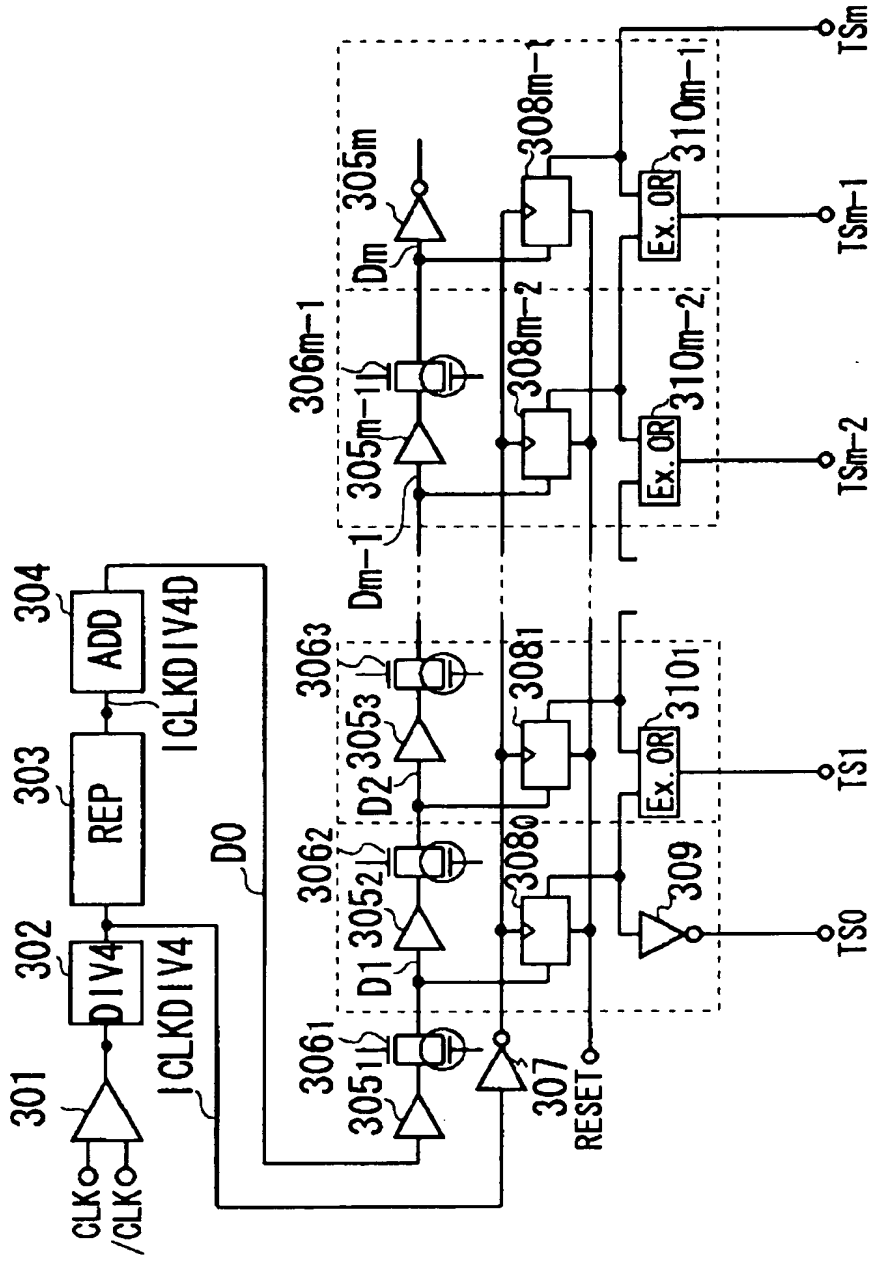

OUT
2010
2040
TS0
2001
2020
2030
2050
2011
TS1
2002
2021
2031
2041
2051
201m-1
TSm-1
200m
202m-1
203m-1
204m-1
205m-1
201m
204m
TSm
VDD
205m
202m
203m
IN

FIG. 2

FIG. 3


CLK
/CLK
301
DIV4
302
REP
303
ADD
304
ICLKDIV4
ICLKDIV4D
DO
3061
3062
3063
3051
3052
3053
D1
D2
Dm-1
Dm
306m-1
305m-1
305m
307
RESET
3081
3082
308m-2
308m-1
308m
309
Ex. OR
3101
310m-2
310m-1
TS0
TS1
TSm-2
TSm-1
TSm

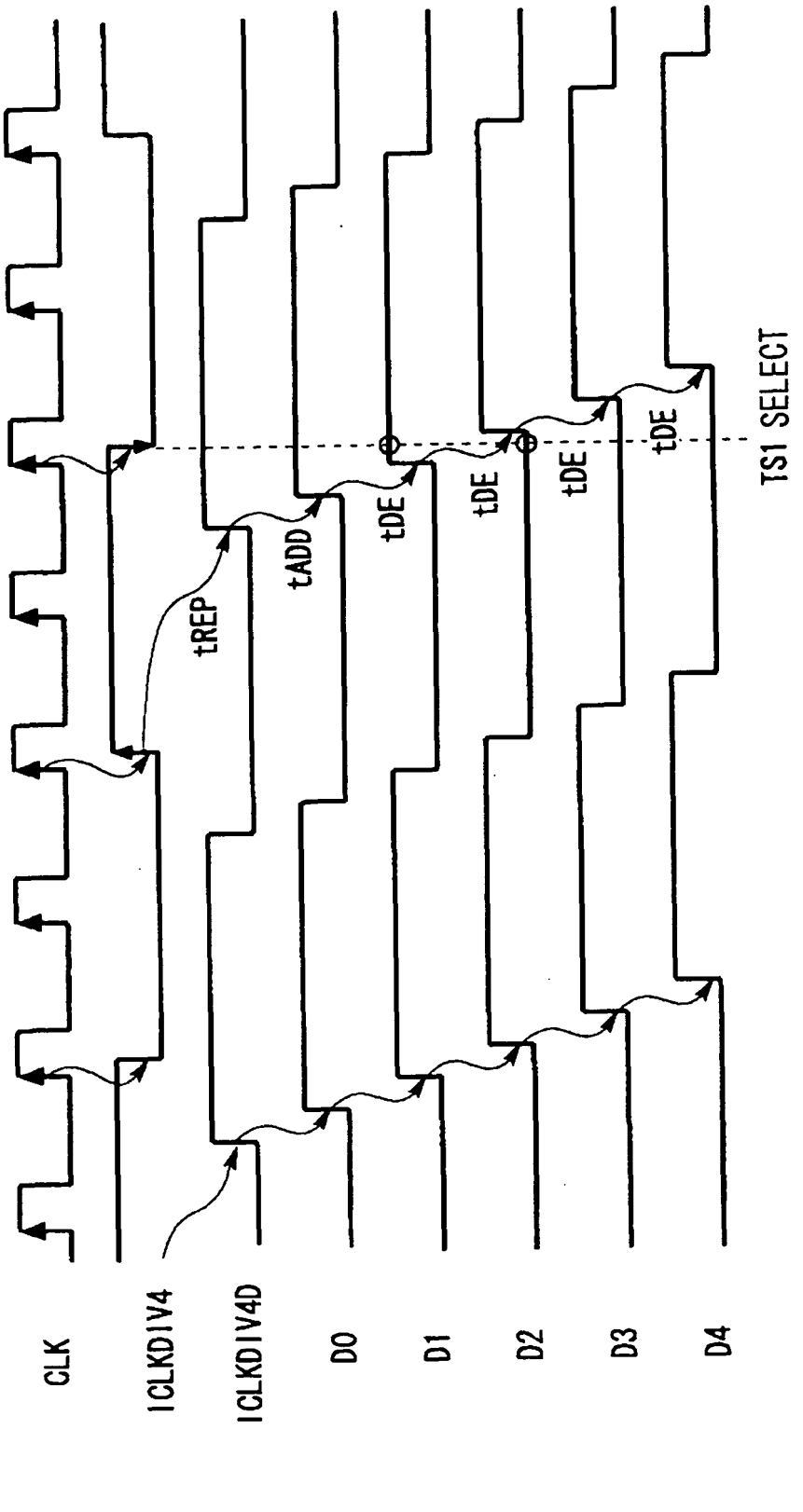

CLK
ICLKD1V4
ICLKD1V4D
D0
D1
D2
D3
D4
tREP
tADD
tDE
tDE
tDE
tDE
TS1 SELECT

FIG. 4

FIG. 5

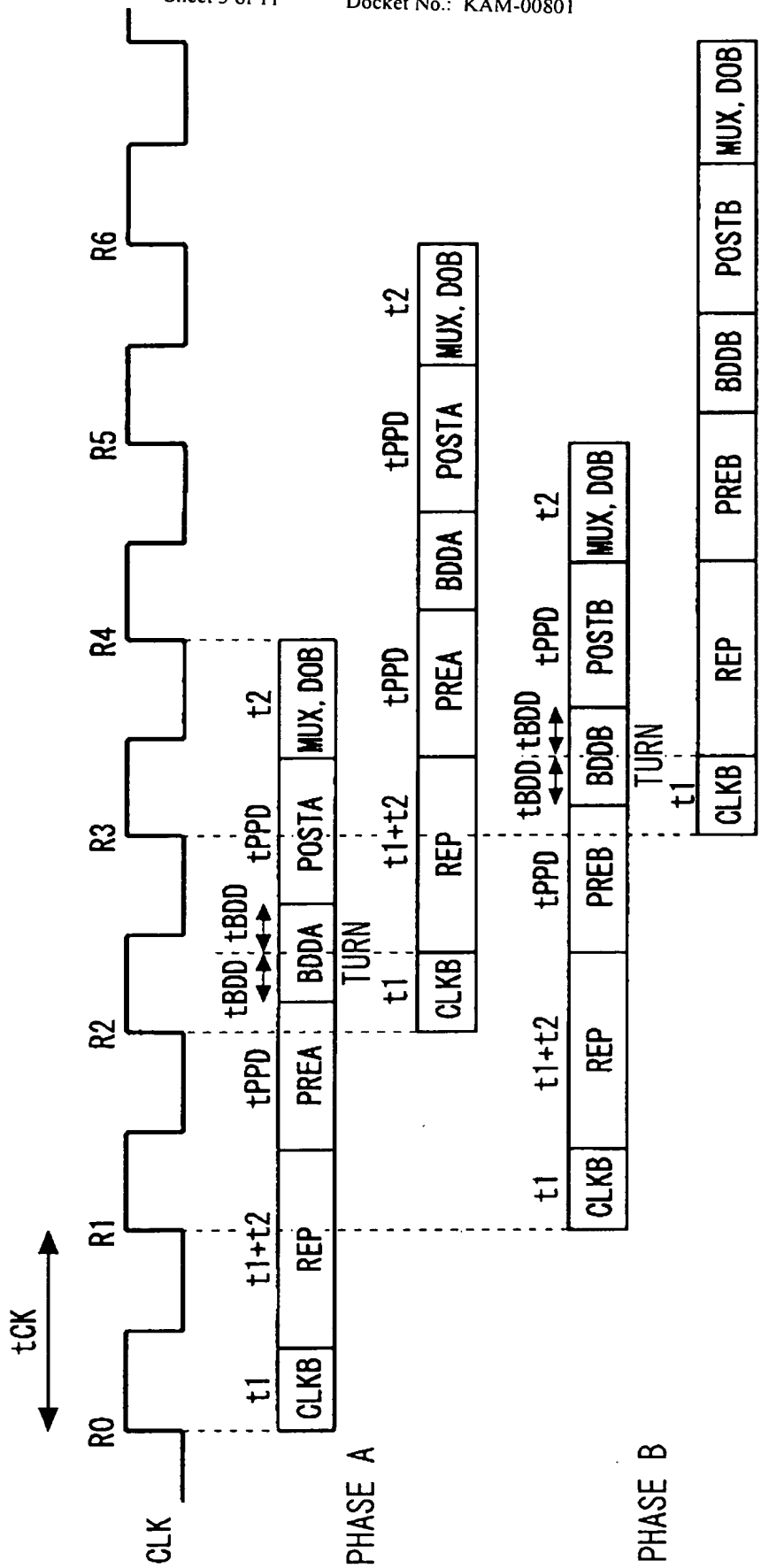
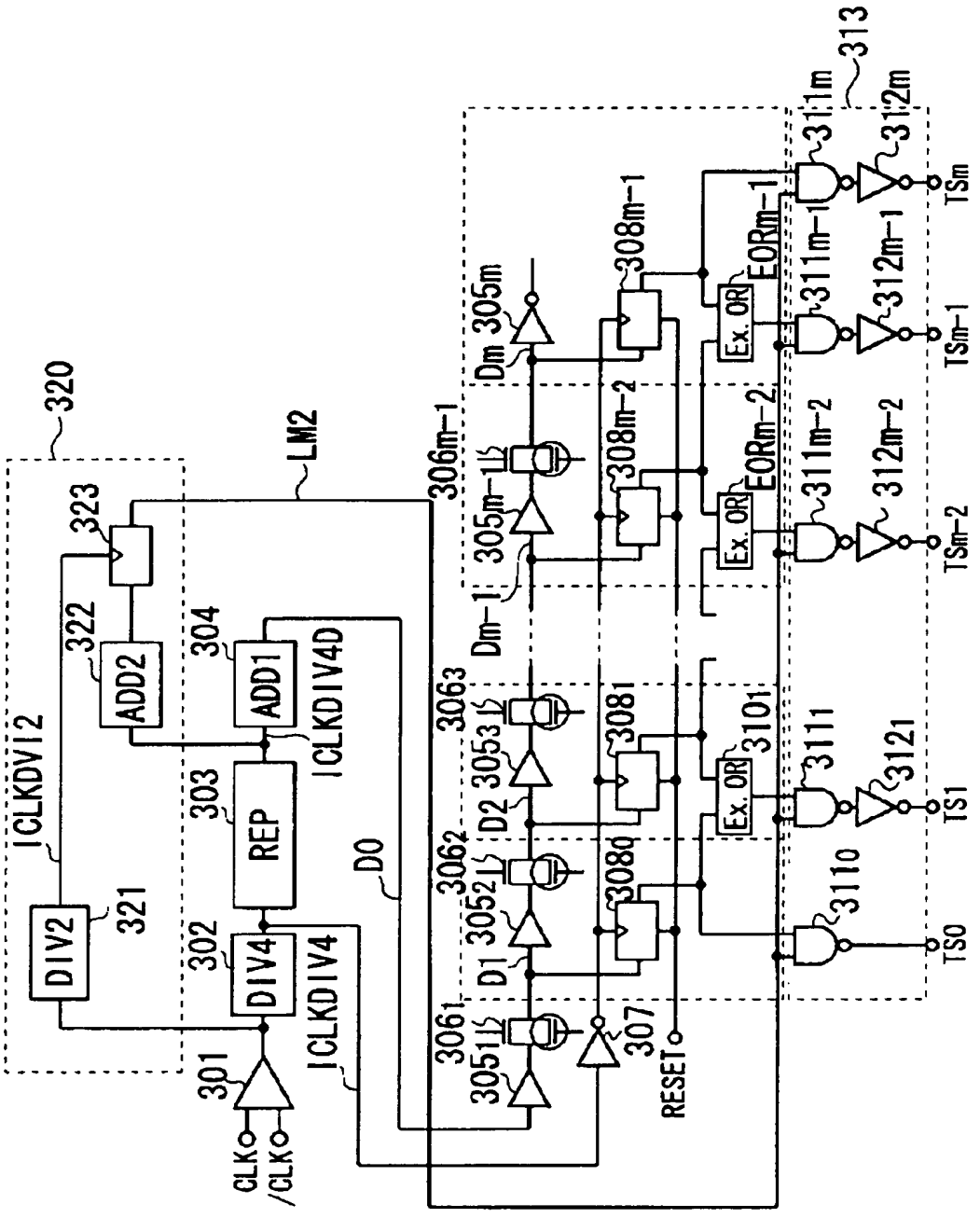

CLK
R0
R1
R2
R3
R4
R5
R6
tCK
t1
t1+t2
tPPD
tBDD
tBDD
tPPD
t1+t2
t1
tPPD
tBDD
tBDD
tPPD
t1+t2
t1
CLKB
REP
PREA
BDDA
POSTA
MUX, DOB
CLKB
REP
PREA
BDDA
POSTA
MUX, DOB
CLKB
REP
PREB
BDDB
POSTB
MUX, DOB
CLKB
REP
PREB
BDDB
POSTB
MUX, DOB
TURN
TURN
PHASE A
PHASE B

FIG. 6


320
LM2
306m-1
313
323
322
ADD2
304
ADD1
ICLKDIV12
ICLKDIV4D
303
REP
DO
ICLKDIV4
DIV2
321
302
DIV4
301
CLK
/CLK
3063
3053
D2
3062
3052
D1
3061
3051
307
RESET
Dm 305m
Dm-1
305m-1
308m-1
308m-2
3081
3080
Ex. OR
EORm-1
EORm-2
3101
311m-1
311m-2
3111
3110
312m-1
312m-2
3121
311m
312m
TSm
TSm-1
TSm-2
TS1
TS0

TITLE: CLOCK SYNCHRONIZATION
CIRCUIT AND SEMICONDUCTOR DEVICE
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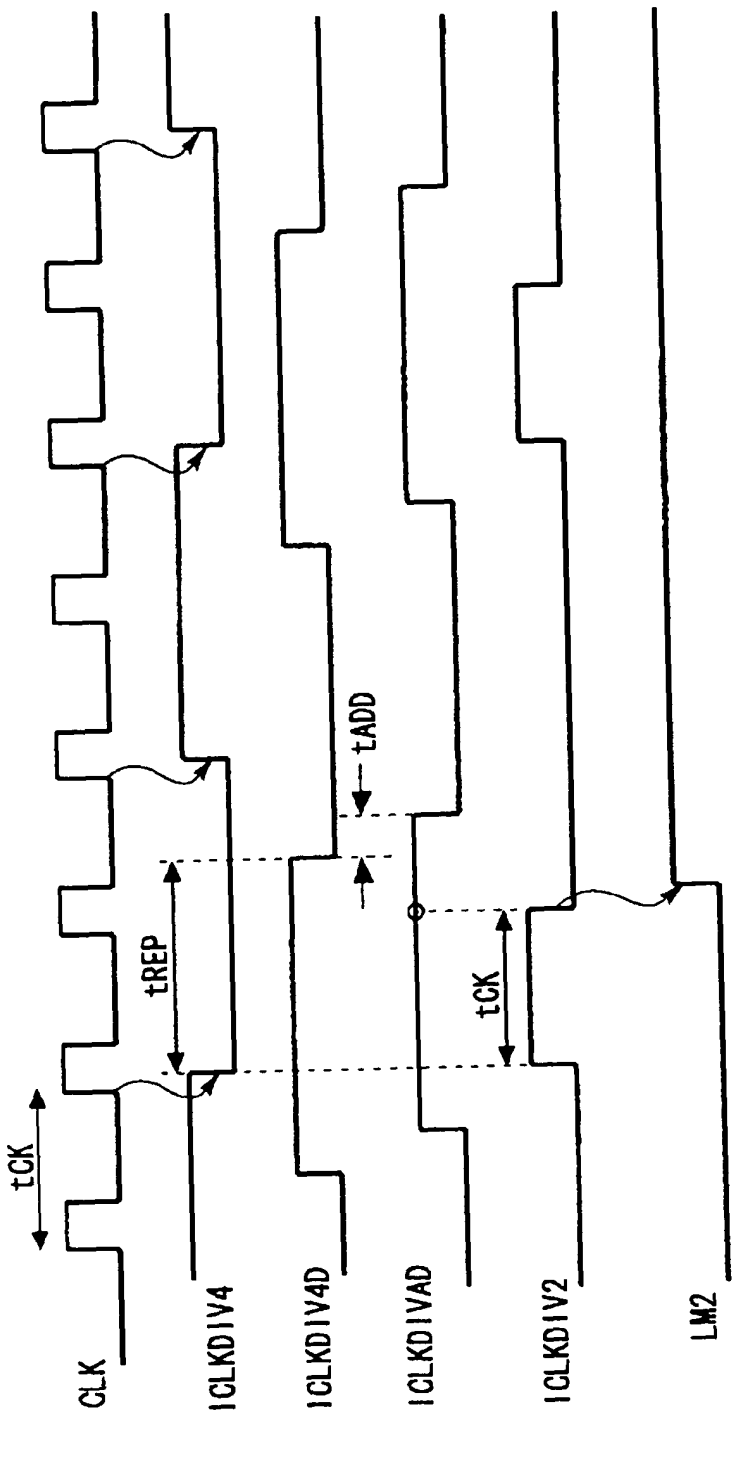


FIG. 7

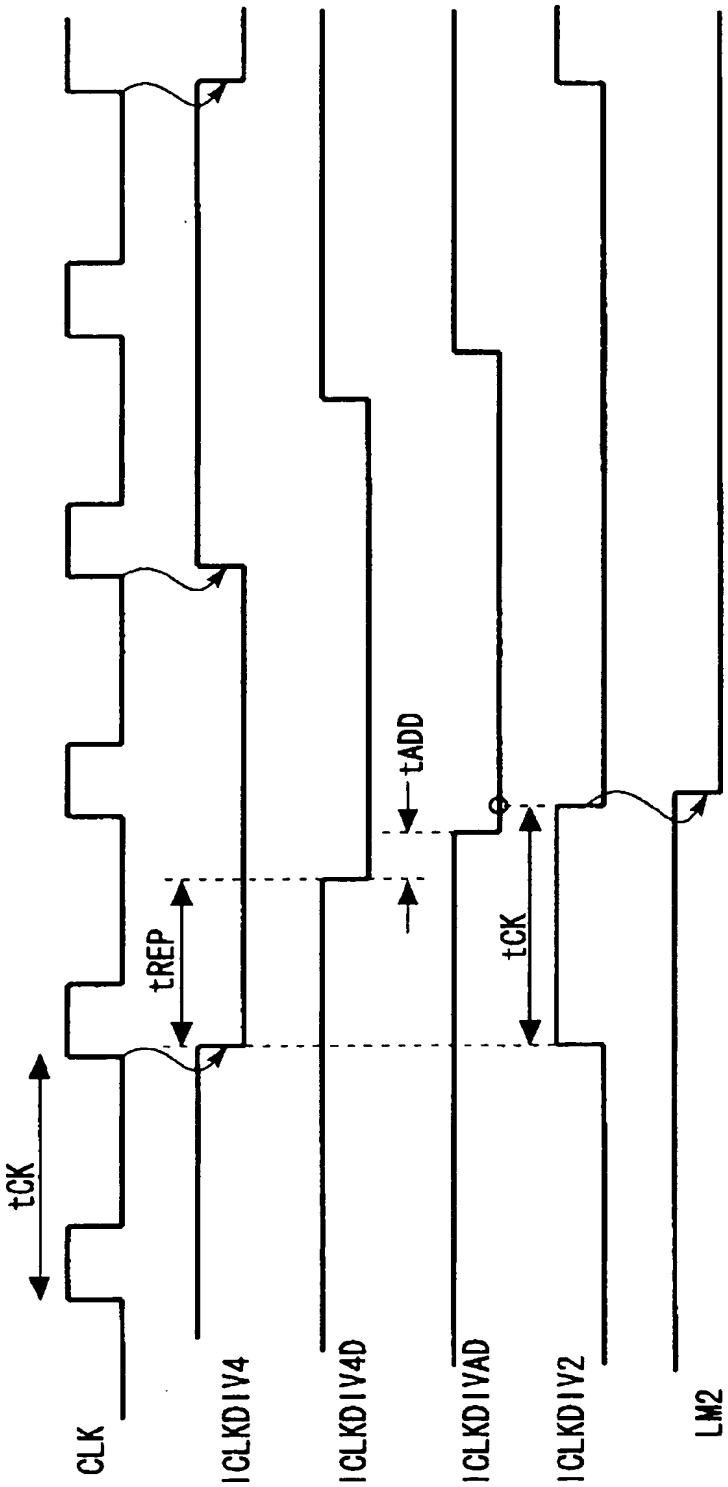

tCK
tREP
tADD
tCK
CLK
ICLKDIV4
ICLKDIV4D
ICLKDIVAD
ICLKDIV2
LM2

FIG. 8

FIG. 9A PRIOR ART

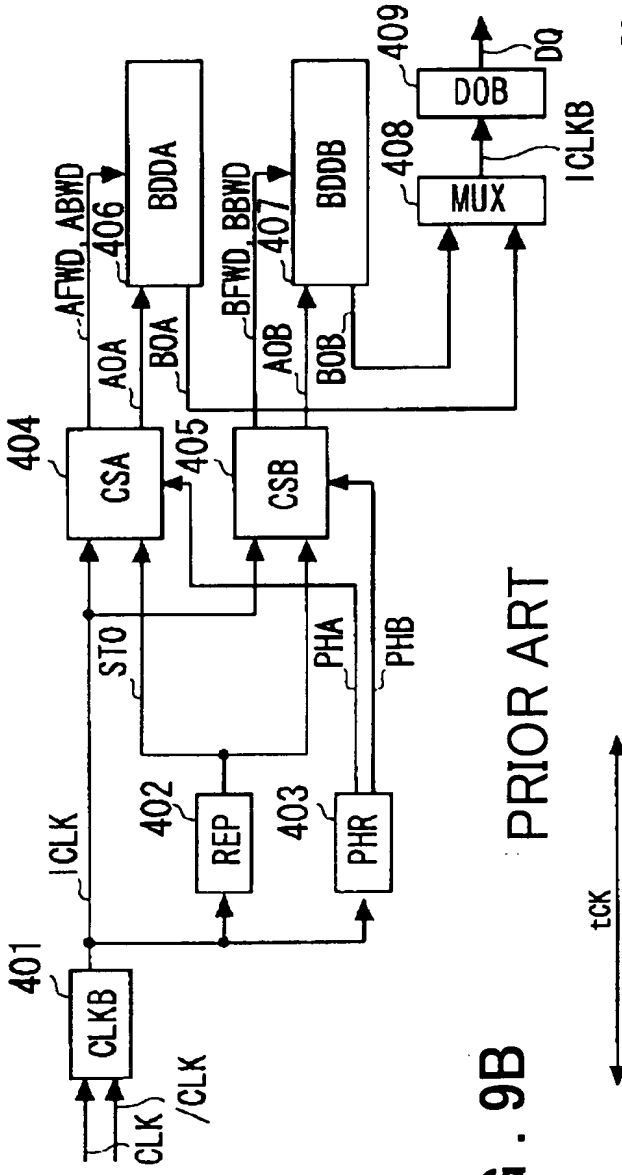
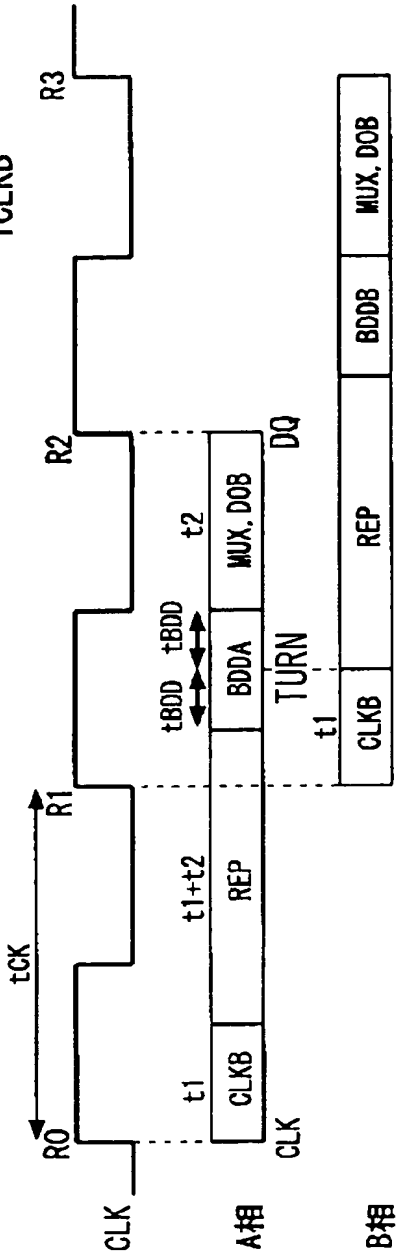


FIG. 9B PRIOR ART



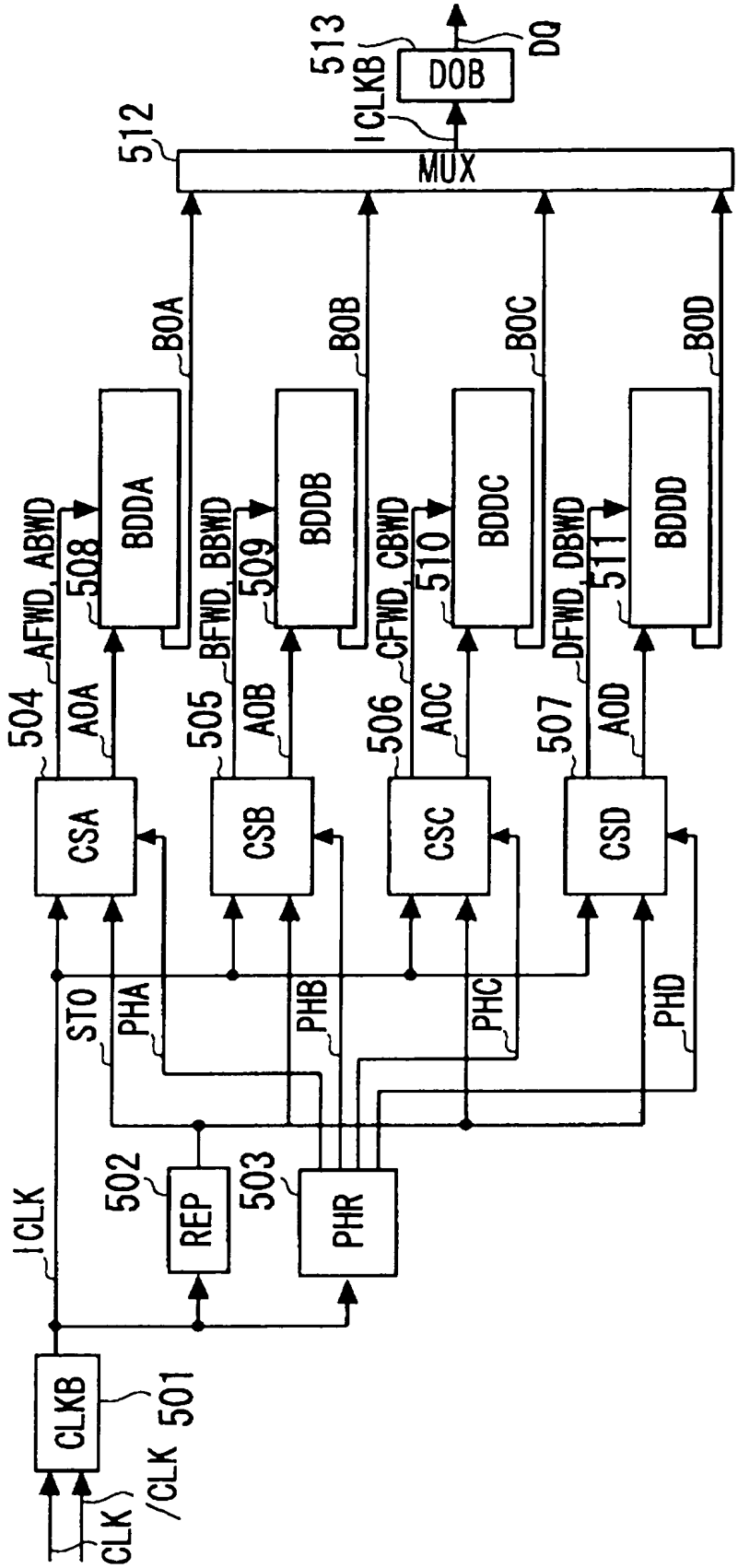


FIG. 10 PRIOR ART

FIG. 11 PRIOR ART